TWO-PHASE HYBRID FLOWSHOP SCHEDULING PROBLEM TO MINIMIZING COMPLETION TIME

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ABSTRACT

In this study, a scheduling problem to minimize total completion time of jobs in an assembly line with two-phase flow shop is considered. In the first phase, there are *m* machines in which different types of parts are manufactured respectively and those *m* parts are assembled at single machine in the second phase. In this problem, until the all parts are not made in the first phase, the second operation could not be proceeded. Also, the second phase should e started immediately when all parts are arrived from the first one due to the quality issue. We formulated this problem as a mathematical form to obtain optimal solution for a small sized problem since this problem is known to be NP-hard. Also, we proposed several heuristic algorithms to solve the large sized problem in a rapid computation time. Simulation study with randomly generated data is conducted to evaluate the suggested methods with optimal solution.

Keywords: scheduling, two-phase flowshop, completion time, hybrid shop

INTRODUCTION

Semiconductor manufacturing companies should satisfy customers' demands in terms of not only quantity and quality but also due dates to survive in competitive business environments. Especially in a FAB which produce multiple types of semiconductor such as application-specific integrated circuits (ASIC), display driver integrated circuits (DDI), Complementary metal oxide semiconductor (CMOS) and so on, meeting quantities of orders on due dates is highly important. Since wafer fabrication is one of the most complex production processes involving hundreds of operations with reentrant flows, it is very important to develop effective and efficient methodologies for making production schedules and controlling material flows to satisfy customers′ demands. In this study, we present scheduling methods that can be used in a semiconductor manufacturing system, for the objective of meeting quantities of customers′ orders while keeping their due dates.

Considering production quantities of forecasting and customers′ orders and due dates of orders, a planning department determines daily quantities of each order to be shipped for several months. Here, this procedure is called product planning (Uzsoy *et al*. 1992a, Uzsoy *et al*. 1992b, Leachman & Carmon 1992). Each order consists of several lots, in which a lot is a unit of transportation and processing and includes 25 wafers. With daily fab-out quantities, scheduler in each workstation decides assignment and sequencing lots to be produced and process of lots are started by the result of dispatcher which shows a lot to be processed on a machine in real time when the machine becomes idle. Here, these workflows are named as scheduling and planning systems in a semiconductor manufacturing fabrication.

If there is no system disturbance, it may be enough to employ results of scheduling system, that includes product planning, scheduler for a certain period of time. However, in real fabrication, unpredictable system disturbances, such as machine breakdowns, operators′ mistakes, system faults and arrivals of urgent orders, occur frequently. Therefore, due to such a dynamic and uncertain nature of the fabrication, there is usually significant gap between planned and real daily fab-out quantities. To cope with the unexpected situation,

real time dispatching systems, in which an idle machine selects a job to be processed, are used. In this real time dispatching system, when a machine becomes idle, a job with the highest priority, which is computed by the implemented rules (Panwalkar & Iskander 1977, Blackstone *et al.* 1982, Kim 1994), is selected to be processed on that machine in real time. However, dispatching rules used in real time dispatching system currently are not effective for compensating for difference between real and planned situation in a fab. In this paper, we suggest scheduling methods for the objective of minimizing the differences between planned and actual production quantities occurred by system disturbances.
In this research, we develop a scheduling method in a semiconductor wafer fabrication that produces multiple product types with different due dates. Since an order has due date, quantity and a product type and, in real FAB, production plan (MP and FP) is constructed to satisfy meeting due date and quantity of order. That is, the daily FAB-OUT quantities of all product types are determined, lots are matched with an order and due dates of lots corresponding to product types are obtained.

ALGORITHM

Here, the followings are notation used throughout the paper.

d_i: due date of lot i
r_i: remaining processing time of lot i
H: considering period from the current day
n: remaining day to FAB-OUT from current day ($\leq H$)
c: current time (to schedule)

H is the predetermined value appropriately by FAB manager who wants to meet FAB-OUT plan in terms of not only quantity but also due date of product. For example, if H is 10 days, he(she) wants to control production process of lot in 10 days from the current day. ri is remaining processing time to complete process of a lot and this can be obtained by using standard processing time in manufacturing execution system. n is the remaining day to FAB-OUT from the current day, however, it should be less than or equal to H. That is, only lots which are planned to complete process in H days are considered in this algorithm.
As described in section of introduction, by factory planning, since the daily FAB-OUT quantity of each product type is given and each lot is corresponded to each product type, each lot has same due date of an order. Priority of lot i (p_i) is computed as

$$p_i = \alpha \times (di - c - r_i) \times (H - n + 1) / H.$$

The first term is the controlling parameter which is determined through many computational experiments. The second term implies the slack time to complete FAB-OUT, that is, if this value is greater than zero, it means that a lot is processed earlier than factory planning. On the other hand, if the term is less than zero, it means that a lot may be tardy and it is necessary to accelerate processing this lot. The third term is a weight of lot. A lot to complete its process today (current day) has maximum weight, i.e. $(H - 0) / H = 1$. Otherwise, a lot to complete its process on the last day of period (H) has minimum weight ($1/H$).
In ascending order of obtained priorities, lots are selected and scheduled, that is, lots with minimum priority should be scheduled first. This suggested algorithm to obtain priorities of lots (of which FAB manager wants to control production process) will be added to a pre-installed area scheduler. Each area scheduler installed in MES gives the schedule results of waiting lots to be processed in each area such as photolithography process, etching process, thin film process and diffusion process. According to the scheduling results, a lot is selected and processed on the machine.

CONCLUSION

This paper focuses the scheduling algorithm that solve problem which is incurred in System LSI wafer FAB. To satisfy the daily FAB-OUT quantity of each product, we develop an algorithm to obtain priorities of lots and will reflect the developed algorithm on FAB scheduler. From the results of the suggested algorithm, it can be expected that not only FAB yield but also customers'satisfaction (by committing due date of orders) are increased.

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